

What is Claimed is:

1        1.    During the testing of the operation of processing  
2    unit, a system for identifying the occurrence of an  
3    interrupt service routine code flush condition in the  
4    pipeline flattener, the system comprising:

5        timing trace apparatus responsive to signals from the  
6    processor unit, the timing trace apparatus generating a  
7    timing trace stream;

8        program counter trace apparatus responsive to signals  
9    from the processing unit, the program counter trace  
10   apparatus generating a program counter trace stream; and

11       synchronization apparatus applying periodic signals to  
12   the timing trace apparatus and to the program counter trace  
13   apparatus, the periodic signals resulting in periodic sync  
14   markers in the timing trace stream and in the program  
15   counter trace stream.

16       wherein the program counter trace apparatus is  
17   responsive to an interrupt service routine code flush  
18   signal, the program counter trace apparatus generating a  
19   sync marker signal group identifying the occurrence of the  
20   interrupt service routine code flush signal and relating  
21   the interrupt service routine code flush signal to the  
22   timing trace stream and to the program code execution.

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24       2.    The system as recited in claim 1 wherein the  
25   marker signal group includes a program counter address, a  
26   timing index and a periodic sync ID.

1  
2       3.   The system as recited in claim 1 further  
3       comprising:

4       data trace apparatus responsive to signals from the  
5   processing unit, the data trace apparatus generating a data  
6   trace stream, wherein the periodic signals are applied to  
7   the data trace apparatus resulting in periodic sync markers  
8   in the data trace stream; and

9       a host processing unit, the host processing unit  
10   responsive to the timing trace stream, the program counter  
11   trace stream and the data trace stream, the host processing  
12   unit reconstructing the processing activity of the  
13   processing unit from the trace streams.

14  
15       4.   The method for communicating an occurrence of an  
16   interrupt service routine code flush signal from a target  
17   processor unit to a host processing unit, the method  
18   comprising:

19       generating a timing trace stream, a program counter  
20   trace stream, and data trace stream, and

21       in the program counter trace stream, including an  
22   interrupt service routine code flush sync marker signal  
23   group indicating an occurrence of an interrupt service  
24   routine code flush signal and relating the occurrence to  
25   the data trace stream and to the timing trace stream.

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27       5.   The method as recited in claim 4 further  
28   including:

1 including periodic sync markers in the timing trace  
2 stream and in the program counter trace stream; and  
3 including in the program code sync marker reference to  
4 a periodic sync marker.

5  
6 6. In a processing unit test environment wherein a  
7 target processor transmits a plurality of trace streams to  
8 a host processing unit, an interrupt service routine code  
9 flush sync marker signal group included in a trace signal  
10 stream, the marker signal group comprising:

11 indicia of the occurrence of an interrupt service  
12 routine code flush signal;

13 indicia of the relationship of the occurrence of the  
14 interrupt service routine code flush signal to the target  
15 processor clock; and

16 indicia of the relationship of the occurrence of the  
17 interrupt service routine code flush signal to the target  
18 processor program execution.

19  
20 7. In a target processing unit generating trace test  
21 signals for transfer to a host processing unit, a program  
22 counter trace generation apparatus comprising:

23 sync marker assembly apparatus, the sync marker  
24 assembly apparatus including:

25 a storage unit;

26 a decoder unit responsive to an interrupt service  
27 routine code flush signal for storing an indicia of the

1 interrupt service routine code flush signal in the storage  
2 unit, the decoder unit generating a controls signal;

3 a gate unit having a timing index, a periodic  
4 sync signal, and a program counter address, the gate unit  
5 storing the timing index, the periodic sync signal and the  
6 program counter address in the storage unit; and

7 a FIFO unit, the storage unit transferring the  
8 stored signals to the FIFO unit in the form of a program  
9 code flush sync marker.

10  
11 8. The program counter trace apparatus as recited in  
12 claim 7 responsive to a selected control signal for  
13 transferring the interrupt service routine code flush  
14 marker in the FIFO unit to an output port of the target  
15 processor.

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17 9. The program counter trace apparatus as recited in  
18 claim 8 wherein the apparatus can form a periodic sync  
19 marker in response to a periodic sync signal.

20  
21 10. The program counter trace apparatus as recited in  
22 claim 9 wherein the interrupt service routine flush signal  
23 indicates the change from a first instruction code sequence  
24 to a second instruction code sequence exiting the pipeline  
25 flattener.

26  
27 11. The program counter trace apparatus as recited in  
28 claim 10 wherein the first instruction code sequence is an

1 interrupt service routine code and the second instruction  
2 sequence is a program code.  
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